GAPMod 1.2

DOCUMENTATION

Rel. 2.2
15-Oct-2019

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Preamble - GAPMod 1.0/1.1 vs. GAPMod 1.2

GAPMod1.2 is essentially identical to GAPMod1.1, with the exception that its footprint has been changed from LGA-type (with 64 small attach pads underneath the module) to “castellated”-type, with 68 attach pads distributed on the periphery of the module (64 pads from GAPMod 1.1 + 4 for future use). This makes SMD assembly more reliable and also allows hand-soldering the module if required. As a result, the order of pins had to be sowhat reshuffled. This is why it might not seem logical at first sight (e.g., pin 51 placed between pins 5 and 6, etc.).

1. Introduction

GAPMod is a core module architectured around GreenWaves Technologies’ GAP8 chip, an ultra-low power Application Processor for the IoT (*Ref[1]).*
GAPMod is intended to facilitate and speed up development of applications around GAP8.
It packs on a small board (*ca.* 26mmx36mm) the “invariant” part of any application based on GAP8 (GAP8 chip, external Flash+RAM memory, associated decoupling caps, crystal oscillator, passives for internal DC-DC, etc.). This core hardware happens to also be, in many use cases, the most demanding part of the overall design in terms of precautions to take and in terms of required PCB technology.

With GAPMod, an application PCB designer can simply drop the module in his/her design and rely on comparatively relaxed Design Rules and reasonably priced PCB technology for his/her own application-specific motherboard.

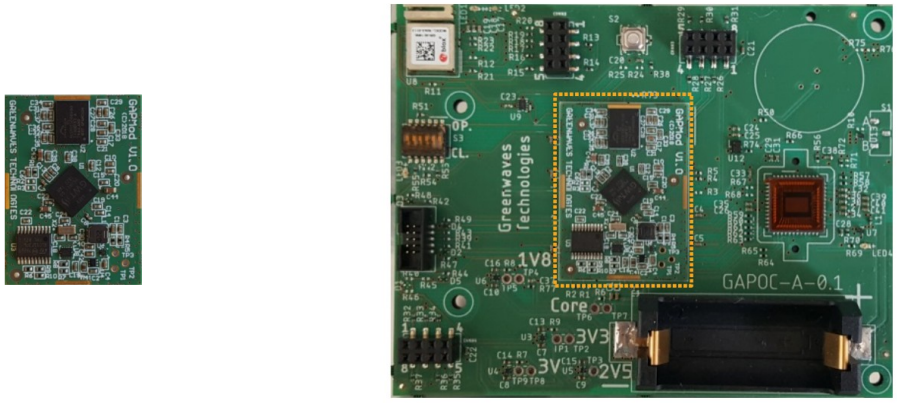

Fig. 1. : GAPMod module, stand-alone (left) and assembled on an application board (right)

2. Board Description

GAPMod comes in the form of a double-sided PCB to be assembled using SMT (Surface Mount Technology) on a target board. All components therefore sit on one side while the other side bears the SMT pads.

All GAP8 I/Os that are not dedicated to interconnecting chips present on GAPMod are made available to the target application board as GAPMod I/Os. For maximum flexibility, power supplies are also to be provided by the application board, with the exception of that dedicated to the on-chip crystal oscillator.
Figure 2 highlights the major parts that constitute GAPMod, while Figure 3 details physical dimensions of the board and location plus size of its I/O pads.

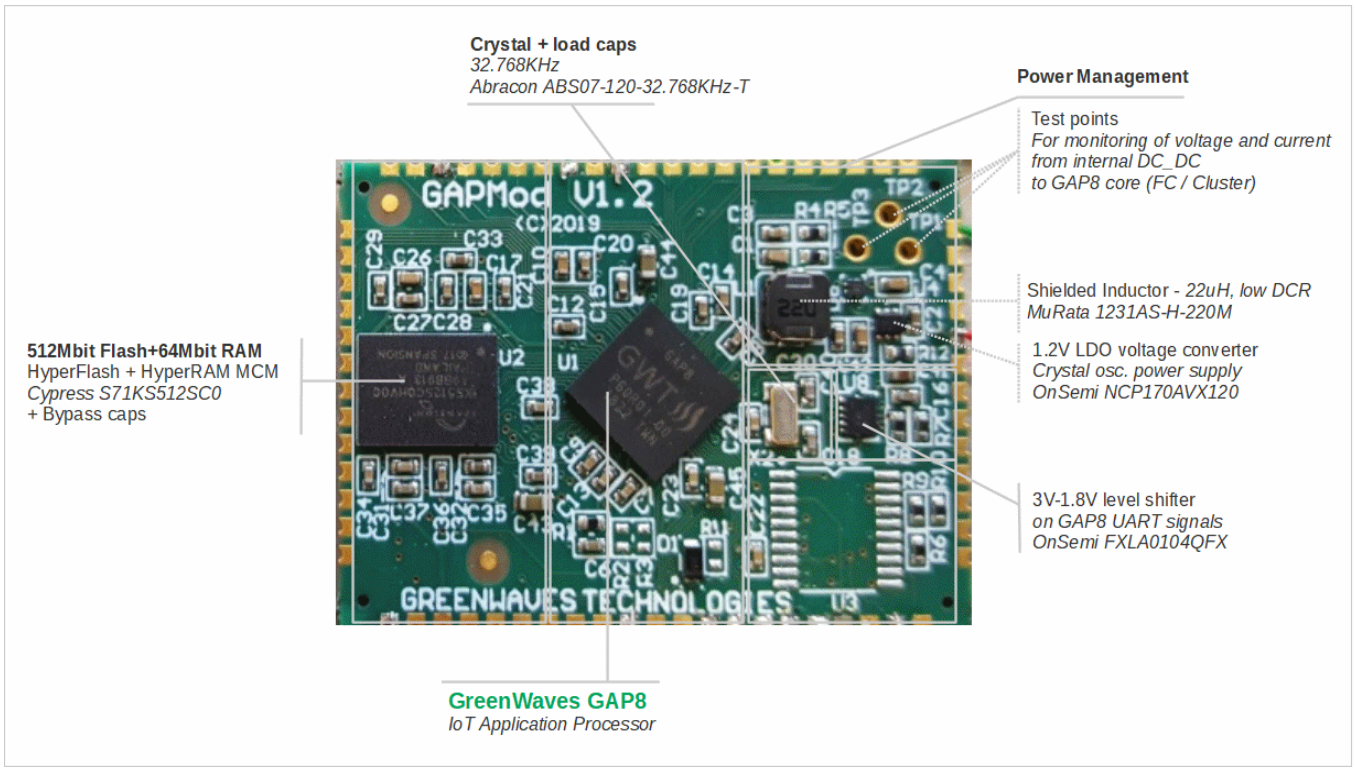

Fig. 2: Anatomy of GAPMod

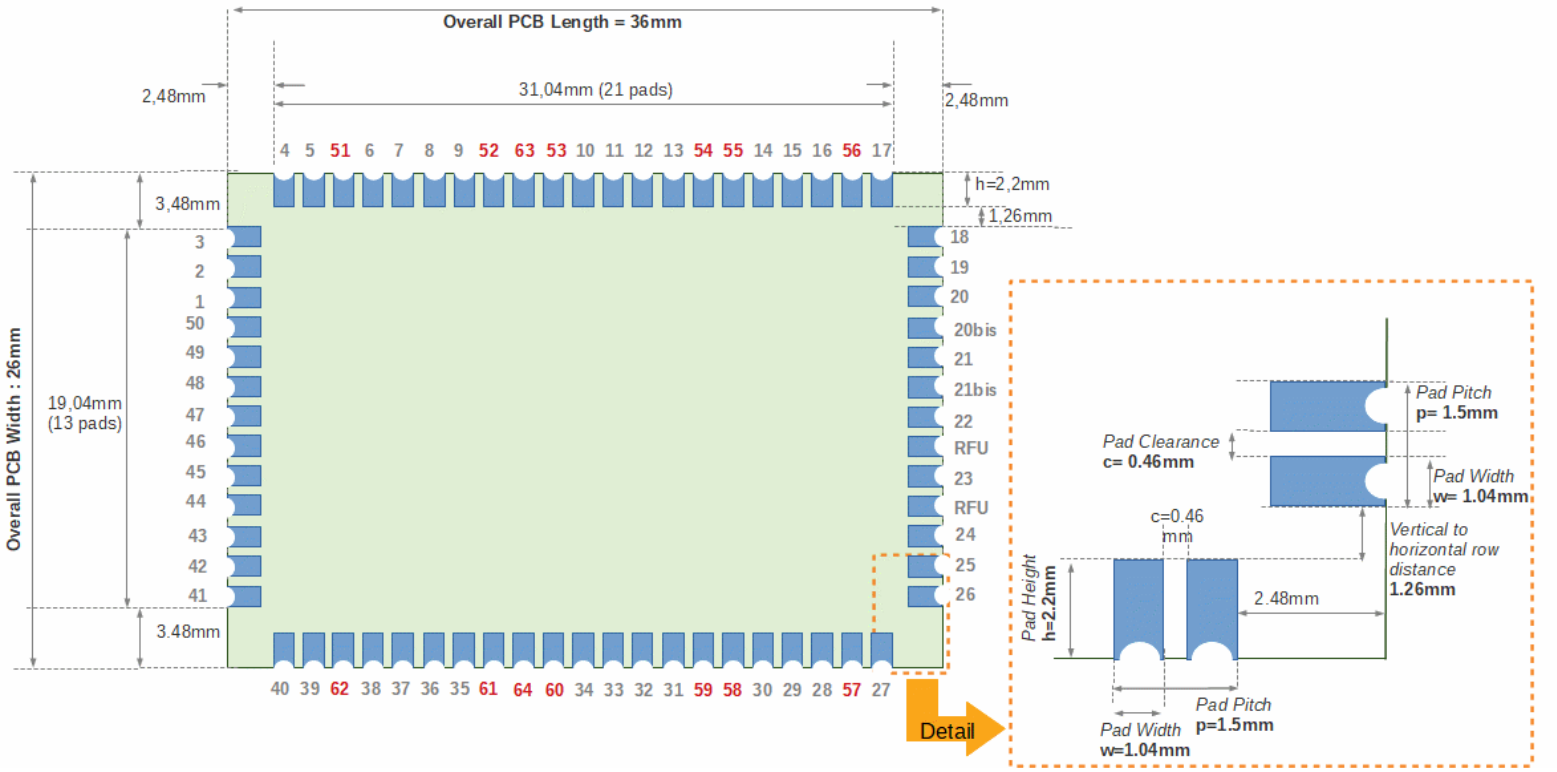

Fig. 3 GAPMod 1.2 Physical Information, TOP (see-through) View

[The occasionally non-consecutive pad numbering allows to keep same [pad # <> function] association between V12 and earlier non-castellated versions]

3. GAP8

Central to the board is the GAP8 chip, an ultra-low power Application Processor for the IoT, bringing intelligence at network edge. GAP8 brings the ability to analyze and classify data from sensors (images, sounds, vibrations etc.) at very low cost and very low power, by extracting from sensor data condensed, meaningful information which can then be sent efficiently over a network.
GAP8 consists on an MCU-like part (a core plus standard peripherals), a processing intensive part (8 identical parallel cores plus a hardware accelerator specialized in Convolutional Neural Network operations), with on-chip L1 and L2 RAM and a specialized DMA. The cores are 32-bit RISC-V enhanced with specialized instructions.
Refer to the GAP8 Product Brief and Datasheet *(Ref.1]) for details.*

4. On-board power management

Refer to Fig. 3 for a graphical illustration of power management on GAPMod.
As mentioned earlier, most power supplies are to be provided by the application board in the sake of flexibility.
However, a 1.2V power supply derived from Vroot (typically battery voltage) is generated on-chip and dedicated to powering the on-chip crystal oscillator. This is to ensure the oscillator, which is quite noise sensitive, always works off a clean and stable power source.

Note also that power supply input “3V_1V8_MEMCORE_MEMIO” goes to the on-board Hyperbus memory and associated I/Os of GAPMod, so its value is dictated by the requirement of this memory chip, i.e. 1.8V (nominal) as GAPMod1.x is normally populated with a Cypress HyperFlash+HyperRAM memory chip in its 1.8V flavor (1.7V min, 1.95V max). However, should there be variants of GAPMod that employ the 3V memory flavor (2.7V min, 3.6V max), then the application board would need to provide 3V rather than 1.8V on input 3V_1V8_MEMCORE_MEMIO.

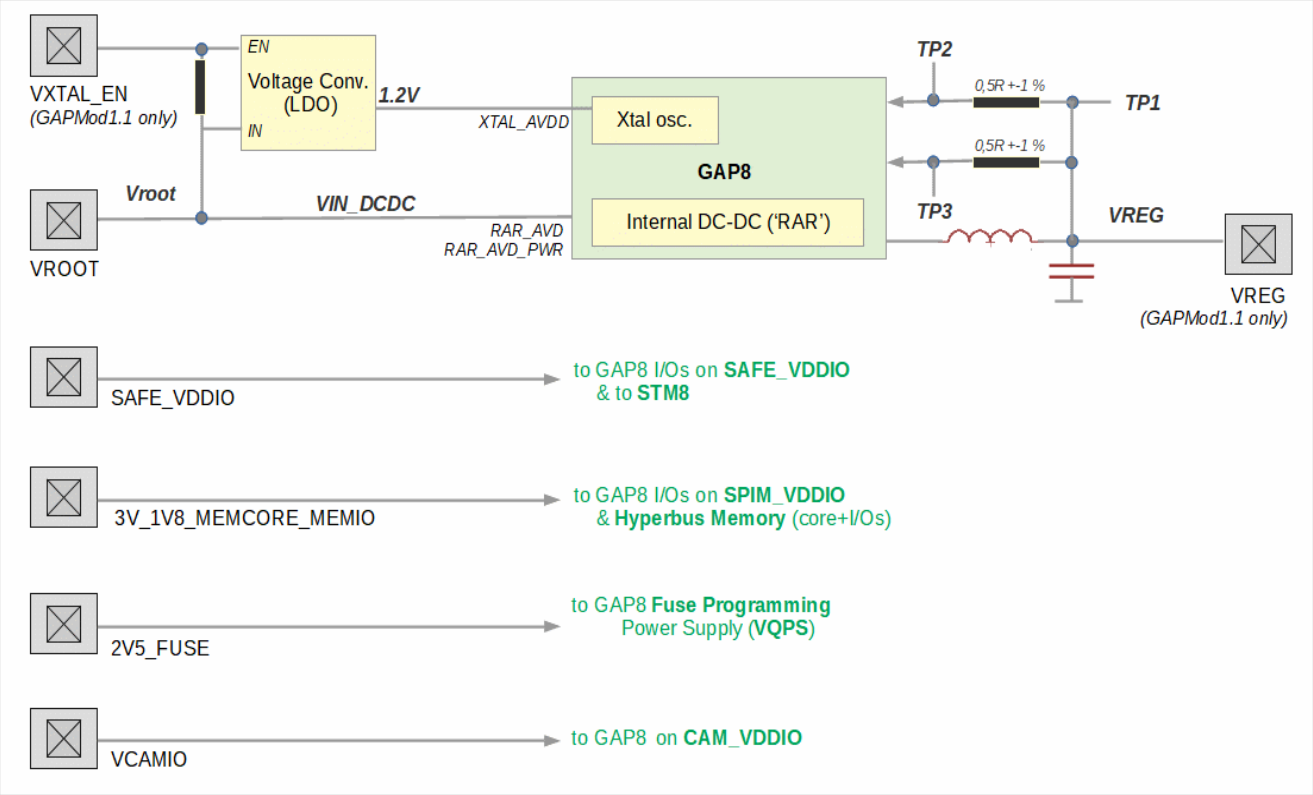

Fig. 3 – On-board power supply generation and control (notional)

– Test Points / Power Supply Monitoring –

3 testpoints are provided to monitor supply voltage and supply currents drawn by the "SoC" part (a.k.a FC, Fabric Controller) of the GAP8 chip and by the "Cluster" part.

> A 0.5 ohm (+-1%) sense resistor placed on the current path **between TP1 and TP2** allows to measure the **current consumption of the SOC region**.

> A 0.5 ohm (+-1%) sense resistor placed on the current path **between TP1 and TP3** allows to measure the **current consumption of the Cluster region**.

The current (in mA) is twice (2x the value of the voltage drop (in mV) measured across the sense resistor (I=U/R). At 0.5ohm, the sense resistor is deliberately small to avoid severe supply voltage fluctuations when there are significant instantaneous current changes.

These currents are measured at output of the DC-DC converter. The efficiency of GAP8's internal DC-DC converter will determine how this translate as actual power drawn by GAP8 for its core (SOC+Cluster).

Note: The efficiency of the DC-DC conversion is impacted by the DC resistance (DCR) of the inductance placed at its output – but lower DCR inductance also means bigger inductance size. On GAPMod the selected inductance has about 300 mOhm maximum DCR, which is very good but requires a somewhat bulky inductance. Other implementations could go for a slightly higher DCR to reduce the footprint of the inductor.

In addition, the regulated voltage VREG is made available on an I/O pad of GAPMod. This allows monitoring VREG; it could be used by external hardware to detect if GAPMod is in Sleep mode without relying on another specific signal, as:
- in normal mode, VREG may range from 1.0V to 1.2V
- in sleep mode, the internal DC-DC switches to LDO mode and provides VREG=0.8V.

Also refer to GAPMod I/O list.

5. HyperBus Memory

GAPMod implements a Flash+RAM MCM (Multi-Chip Module), employing Cypress's HyperBus specification (*Ref[2])*. The selected part is Cypress's S71KS512SC0B, offering 512Mbit of Flash and 64Mbit of RAM and using 1.8V nominal power supply (1,7V min, 1,95V max).
It might happen that future versions of GAPMod employ different variants of Cypress HyperBus memory (e.g. Flash only, or 3V rather than 1.8V power supply, or different capacity). These are pinout-compatible and GAPMod's architecture allows to perform with swap without any other board hardware change.

6. Programming / Debugging

Code can be downloaded into GAP8 internal RAM or into the Hyperbus Memory present on GAPMod through its JTAG interface. This is done using the **standard GAP8 SDK**, please refer to its documentation *[Ref.3].*

7. GAPMod I/O Signal Assignements

Please refer to Table "GAPMod I/Os" (provided as a separate spreadsheet ([*Ref.4]*).

REFERENCES

Ref[1] -
Product Brief "*GAP8 IoT Application Processor*" – available from *greenwaves-technologies.com*
DataSheet "*GAP8 Hardware Reference Manual*" – available from *greenwaves-technologies.co*m

Ref[2] -
"HyperBus specification – Low signal Count, High Performance DDR Bus"
"HyperFlash and HyperRAM Multi-Chip Package 1.8V/3V"
www.cypress.com/products/hyperbus-memory

Ref[3] -
GreenWaves GAP8 SDK & Manuals : *greenwaves-technologies.com/en/sdk/*

Ref[4] -
Functional Definition of GAPMod 1.x I/Os :
Spreadsheet *GAPMod_v1.x_IO_Definition.xlsx* available from GreenWaves
Pin # on GAPMod vs. connection of GAPMod (e.g. Pin ID on GAP8 if relevant) and brief description of intended usages.

DOCUMENT HISTORY

Draft A – Dec.2018 (XC)
Initial Draft

Draft B – 17-Jan-2019 (XC)
Added Disclaimer & License type

Rel. 1.0 – 23-Apr-2019 (XC)
Changed marking from Draft to Rel.1.0

Rel. 1.1 – 5-Jun-2019 (XC)
Added note about current consumption.

Rel. 2.0 – 2-Jul-2019 (XC)
Distinction between GAPMod 1.0/1.1 (LGA-style pinout) and GAPMod 1.2 (castellated pinout).

Rel. 2.1 – 22-Aug-2019 (XC)
Added a clarification regarding pad numbering in GAPMod 1.2

Rel. 2.2 –15-oct-2019 (XC)
Dedicate doc to GAPMod 1.2